**Lab 2 – Designing a 4-bit binary Adder-Subtractor using Xilinx Vivado**

CECS 341 – Computer Architecture & Organization

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**Goal/Objective:**

The goal of this lab is to use the knowledge learned from lab one to design a 4-bit adder or subtractor by using Xilinx Vivado.

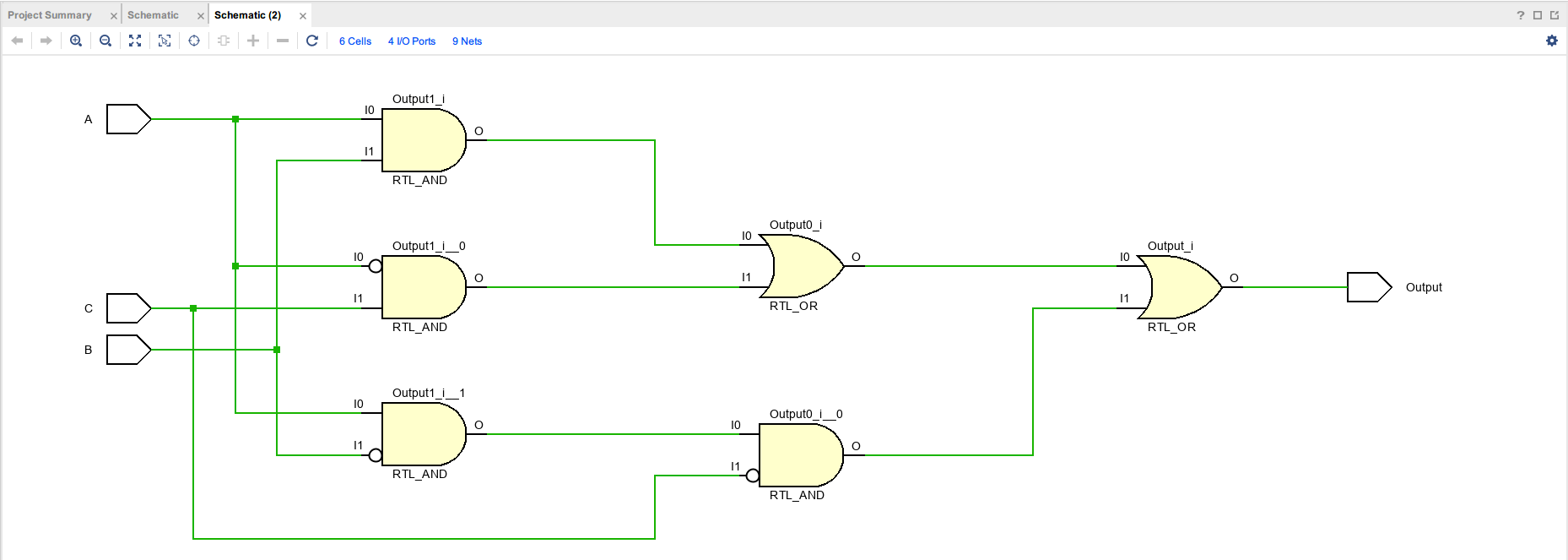
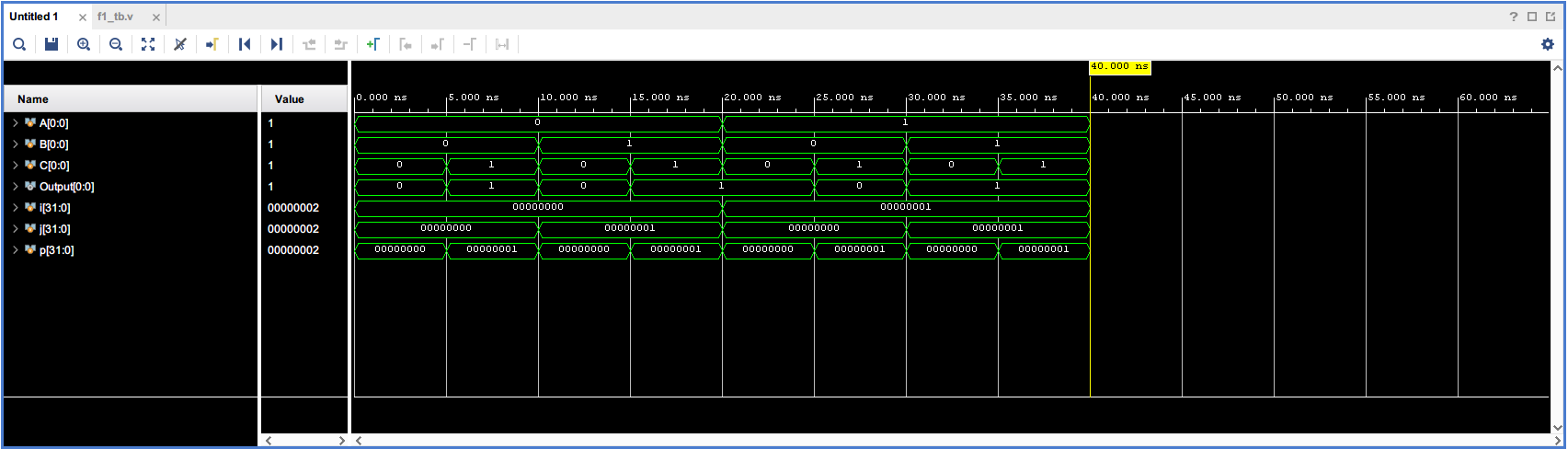
**Technical Description/Steps:**

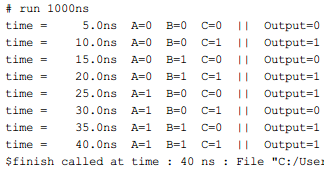
In part one, we use our knowledge from class to design two circuits that utilize operators to produce desired outputs. We create a test bench for these two circuits to see if they work properly.

In part two, we use the full adder to build a 4-bit adder/subtractor in Vivado. First, we create multiple inputs and wires such as “Carry\_in” and “Sum” to connect all four full adders. We use the XOR gate operator that connects to input “B” and “K” to determine addition or subtraction. After that, we create a test bench to see if the 4-bit adder/subtractor works.

**Results:**

Part 1 Circuit 1:



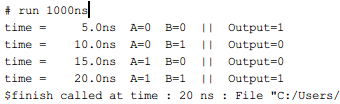
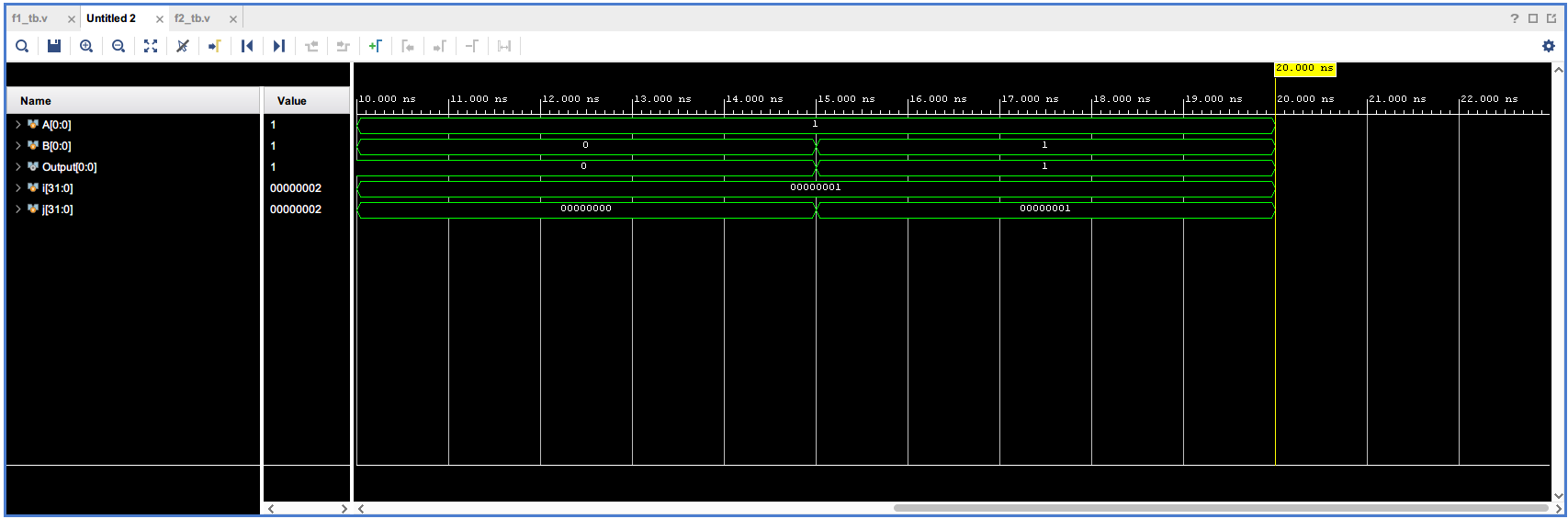


The schematic of circuit one shows that the inputs need to go through the NOT gates, AND gates, and OR gates to get the output. The waveform and results in the console show the circuit runs perfectly.

Part 1 Circuit 2:

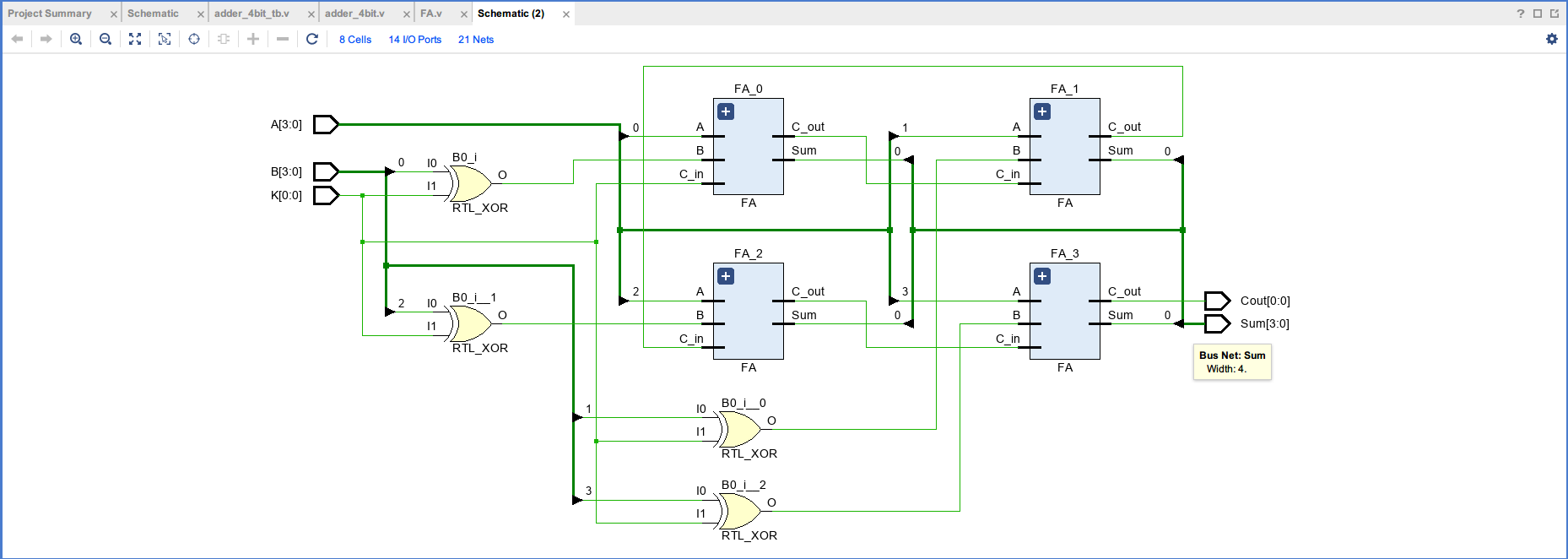
Diagram

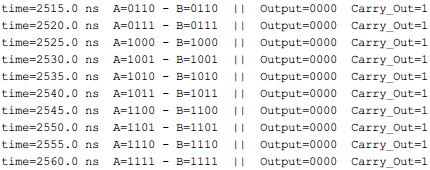
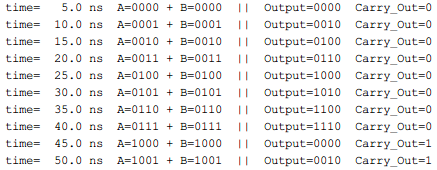
Description automatically generated with medium confidence



Just as in the schematic of circuit one, the schematic of circuit two shows input A and B go through NOT gates, AND gates, and OR gates to produce the output. The waveform and console output demonstrate that the circuit works as intended.

Part 2:



Graphical user interface

Description automatically generated

The schematic of part two shows that input A is connected to all four of the full adders, while input B and input K are connected to an XOR gate to determine addition or subtraction. The output of the XOR gates is connected to the full adders to produce the final product and carry. The waveform and the results in the console show the circuit functions as intended as a 4-bit adder/subtractor.

**Conclusion:**

After this lab, our knowledge in working with Vivado has strengthened. We feel more confident in connecting inputs to modules and assigning outputs. In addition, we feel more sure in writing test benches.

We encountered some difficulties in creating the XOR gates in part two. After some research in the PowerPoint posted by the professor, we realized that we could use the XOR operator to accomplish this job.